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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,040	08/23/2001	Mark Hatzilambrou	IME00-015	1682

28112 7590 08/06/2003

GEORGE O. SAILE & ASSOCIATES
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER
KITOV, ZEEV

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 08/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,040	HATZILAMBROU ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8, 10, 26 - 33* is/are rejected.

7)☒ Claim(s) *9, 11 - 25, 34, 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Drawings

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. Objection

a) Claims 4 and 29 are objected to due to a following statement: "said power shunt circuit is in close proximity to said one or more I/O pads by providing one of said power shunt circuits per said pair of power supply rails" (emphasis added). The sentence in a whole does not make a sense because it implies some connection between close proximity of the shunt circuit to the I/O pads and providing one of power shunt circuits per pair of power supply rails. Such connection is not disclosed in the Specification, neither in Drawings. For purpose of examination the statement is interpreted as follows: "said power shunt circuit is in close proximity to said power supply rails thus providing one of said power shunt circuits per said pair of power supply rails".

b) Claim 8 is objected to because the Claim recites a limitation "said CMOS inverter" on page 20, line 1. There is insufficient antecedent basis for this limitation in the claim.

c) Claim 9 is objected to due to a following statement: " width ratio between said fifth PMOS transistor and said second NMOS transistor of about 4:1, respectively" (emphasis added), which does not make a sense. For purpose of examination the sentence was interpreted as follows: "width ratio between said fifth PMOS transistor and said first NMOS transistor of about 4:1, respectively".

d) Claim 22 is objected to because the Claim recites a limitation "said dimension S". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A reason for that is that according to a claim language, "a fourth PMOS transistor having its source and drain coupled to said second power supply rail and having its drain coupled to said node A" (emphasis added). If it is true, the node A is grounded and the circuit cannot function, as claimed. For purpose of examination, it was interpreted as: "its gate coupled to said node A".

3. Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

a) Claims 26 – 28, 30 - 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker (US 5,744,842) in a view of Saleh (US 5,991,135). Ker discloses many elements of the claim including a dual-mode shunt system providing a low impedance path for ESD, the dual-mode shunt system comprising a first and a second power supply rail (elements Vdd and Vss in Fig. 9) connected to a power supply; a transient-type power shunt circuit connected to the first and said second power supply rail (element 100 in Fig. 9), including timer and driver circuits (elements C and R in Fig. 9), the power shunt circuit providing a low impedance path for an ESD between the first and said second power supply rails and is designed to turn on when the voltage ramp on the first power supply rail is faster than a RC time-constant (of elements R, C in Fig. 9), and larger than the threshold voltage (Vt) of a transistor (elements 100 and 104 in Fig. 9). It further discloses a first and a second I/O diode formed in-between the first and said second power supply rails (shown connected to Input Pad in Fig. 9), the junction of said first and said second I/O diode coupled to an I/O pad, the first and said second I/O diode providing a conductive path for the ESD. As to a claimed PMOS transistor, it is well known in the art, that the PMOS and NMOS transistors are mutually replaceable by simply mirroring the driver circuit, such as swapping R and C elements.
However, Kerr does not disclose a plurality of ESD protection elements used with plurality of power supplies. Saleh discloses a plurality of the ESD protection circuits with multiple supplies. Each input in his system is protected by two ESD devices, which according to him (col. 6, lines 4 –24) may be implemented with P+/well or N+/substrate

diodes. It further discloses additional protection circuit across power supply terminals of individual circuits (circuit 1, circuit 2 and circuit 3 in Fig. 3). Therefore, he discloses a dual-mode ESD protection system. As to a shunt device, according to Saleh (col. 6, lines 4 – 24), the protection element 90 connected across power terminals of the circuits may be implemented with grounded gate NMOS, diode connected PMOS or NMOS transistors; each of the listed solutions is a shunt circuit. He further discloses the plurality of the dual-mode shunt systems capable of operating at any voltage of the power supplies, which are isolated from each other. Both patents have the same problem solving area, namely providing the ESD protection for semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker solution according to Saleh by assigning the dual-mode ESD protection circuit for circuit block fed by individual power supplies, because as Saleh states (col. 1, lines 62 –67, col. 2, lines 1 – 21), for ESD protection of the multiple power supply system there must be protection structures incorporated between all power and ground supply rails (in addition to protection circuitry within any circuit block) to guard against damage caused during any ESD stressing between the terminals of different circuit blocks with unrelated power rails.

Regarding Claims 27 and 28, Saleh discloses the plurality of said dual-mode shunt systems coupled together via the second power supply rails (line connecting upper terminals of elements 62, 64 and 66 in Fig. 3), each of said second power supply rails coupled to another second power supply rail (line connecting bottom terminals of elements 62, 64 and 66 in Fig. 3) below elements by means of a set of complementary

polarity diodes (elements 62, 64 and 66 in Fig. 3), isolating the plurality of second power supply rails from each other and limiting power supply noise cross talk (col. 2, lines 64 – 67, col.3, lines 1 – 30). As a result of use of complementary polarity diodes between the second power supply lines, the voltage between any of the plurality of second power supply lines does not differ by more than one diode drop.

Both patents have the same problem solving area, namely providing the ESD protection to the semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker circuit according to Saleh, because as Saleh states (col. 1, lines 56 – 61, col.3, lines 22 – 30), in analog or mixed signals circuits, the voltage supplies may be different, and therefore, it is desirable to impede digital noise from reaching the analog circuit.

Regarding Claim 29, Ker discloses the shunt circuit being in close proximity to the power supply lines (col. 10, lines 29 – 45). An evidence for that is in disclosed dimensions of the ESD protection circuit. Ker further discloses providing one of the shunt circuits (element 100 in Fig. 9) per the pair of power supply rails (seen in Fig. 9).

Regarding Claims 30 and 31, Saleh discloses P+/N-well diodes (col. 2, line 50). As well known in the art, such a structure is made in an N-well/P-substrate process. He further discloses N+/P-substrate diodes (col. 2, line 50). When the latter solution is used, the substrate becomes one of the diode terminals, and therefore, connection of the second supply line to the substrate is an inherent step in the manufacturing process. Both patents have the same problem solving area, namely providing the ESD protection to the semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill

in the art at the time the invention was made to have implemented the Ker circuit by using the manufacturing process according Saleh, because it is a common solution widely used in the semiconductor industry.

Regarding Claim 32, Saleh discloses plural I/O pads (elements 54, 56 and 58 in Fig. 3) coupled via their own first and second I/O diodes (elements 90 in Fig. 3) to the first and second power supply rails. Both patents have the same problem solving area, namely providing the ESD protection to the semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used additional I/O protection diodes connected to each of the I/O pads in the circuit of Ker, because protecting the I/O pads with the diodes was disclosed by Ker, and repeating the same solution for the additional I/O pads is mere multiplication of the essential working parts of the device, which involves only routine skill in the art.

Regarding Claim 33, Ker discloses the power shunt circuit having the timer circuit connected to the driver circuit (elements 102 and 100 in Fig. 9) the timer and driver circuits utilizing metal oxide semiconductor (MOS) switching devices coupled between the first and said second power supply rail.

b) Claims 1 - 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker (US 5,744,842) in a view of Saleh and further in a view of Ker et al. article in IEEE Journal of Solid-State Devices.

Claim 1 differs from Claim 26 by its limitation requiring the dual diode scheme ensuring that the capacitance of the I/O pad is bias independent for RF signal inputs. As was stated above, over Ker and Saleh disclose all the elements of Claim 26. Regarding Claim 1, Ker et al. article discloses the dual diode scheme (elements Dp1 and Dn1 in Fig. 7) ensuring that the capacitance at said I/O pad is bias independent for RF signal inputs (pages 1197 - 1198, part B. Input Capacitance). Both references have the same problem solving area, namely providing the ESD protection for semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified solution of Ker in accordance with teachings of Ker et al. article, because as Ker et al. state (page 1195, col. 1, lines 1 – 16), for some high precision circuit operations, the input capacitance of an analog input is required to be kept as constant as possible within the input voltage swing range.

Regarding Claims 2 and 3, Saleh discloses the plurality of said dual-mode shunt systems coupled together via the second power supply rails (line connecting upper terminals of elements 62, 64 and 66 in Fig. 3), each of said second power supply rails coupled to another second power supply rail (line connecting bottom terminals of elements 62, 64 and 66 in Fig. 3) below elements by means of a set of complementary polarity diodes (elements 62, 64 and 66 in Fig. 3), isolating the plurality of second power supply rails from each other and limiting power supply noise cross talk (col. 2, lines 64 – 67, col.3, lines 1 – 30). As a result of use of complementary polarity diodes between the second power supply lines, the voltage between any of the plurality of second power supply lines does not differ by more than one diode drop.

Regarding Claim 4, Ker discloses the shunt circuit being in close proximity to the power supply lines (col. 10, lines 29 – 45). An evidence for that is in disclosed dimensions of the ESD protection circuit. Ker further discloses providing one of the shunt circuits (element 100 in Fig. 9) per the pair of power supply rails (seen in Fig. 9).

Regarding Claims 5, 6 and 21, Saleh discloses P+/N-well diodes (col. 2, line 50). As well known in the art, such a structure is made in an N-well/P-substrate process. He further discloses N+/P-substrate diodes (col. 2, line 50). When the latter solution is used, the substrate becomes one of the diode terminals, and therefore, connection of the second supply line to the substrate is an inherent step in the manufacturing process. Both patents have the same problem solving area, namely providing the ESD protection to the semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented the Ker circuit by using the manufacturing process according Saleh, because it is a common solution widely used in the semiconductor industry.

Regarding Claim 7, Saleh discloses plural I/O pads (elements 54, 56 and 58 in Fig. 3) coupled via their own first and second I/O diodes (elements 90 in Fig. 3) to the first and second power supply rails. Both patents have the same problem solving area, namely providing the ESD protection to the semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used additional I/O protection diodes connected to each of the I/O pads in the circuit of Ker, because protecting the I/O pads with the diodes was disclosed by Ker,

and repeating the same solution for the additional I/O pads is mere multiplication of the essential working parts of the device, which involves only routine skill in the art.

c) Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker in a view of Saleh, Ker et al. article in IEEE Journal of Solid-State Devices and further in a view of Voldman (US 6,404,269). Ker discloses most of the elements of the claim including a fourth PMOS transistor (element 200 in Fig. 11) having its source and drain coupled to said second power supply rail and having its gate coupled to the node A (marked Vx in Fig. 11), the fourth PMOS transistor wired to function as a capacitive means, the resistive means together with the fourth PMOS transistor acting as said RC time-constant; a CMOS inverter driver, formed by a fifth PMOS transistor (element Mp in Fig. 11) and a first NMOS transistor (element Mn in Fig. 11) coupled in series, such that the source of the fifth PMOS transistor is coupled to the first power supply rail and the source of the first NMOS transistor is coupled to the second power supply rail, the junction of the fifth PMOS transistor and the first NMOS transistor coupled to a node D (marked as Vb in Fig. 11), and the gate of the fifth PMOS transistor and the first NMOS transistor coupled to the node A, the CMOS inverter driver providing drive current; and a second NMOS transistor (element 100 in Fig.11), its drain and source coupled between the first and the second power supply rail, respectively, and the gate of the second NMOS transistor coupled to the node D, the second NMOS transistor shunting an ESD from the first power supply rail to the second power supply rail. However, it does not disclose the first, the PMOS transistors acting as a resistive means. Voldman discloses

PMOS transistors (elements 200 and 201 in Fig. 6, col. 7, lines 37 - 52) having their gates connected to the second power supply (Vss in Fig. 6) and acting as a resistive means. Both patents have the same problem solving area, namely providing the ESD protection to the semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker circuit by using the resistive PMOS transistors according to Voldman, because it is widely used method in a modern semiconductor technology.

Regarding Claim 10, Ker et al. article in IEEE Journal, discloses an NMOS transistor having width/length dimension of about 2000/0.35 microns, respectively (page 1196, col. 2, lines 2 –4). Both references have the same problem solving area, namely providing the ESD protection to the semiconductor IC's. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker circuit by using a teaching of Ker et al. article, because as Ker et al. states (page 1196, col. 2, lines 2 –4), it is essential for the circuit ability to withstand a high ESD level.

4. ***Allowable Subject Matter***

Claims 9, 11 –25, 34 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is as follows.

Regarding Claim 9, the claim states, inter alia, that said CMOS inverter driver has its trip point skewed high to speed the turn-on of said second NMOS transistor by selecting a width ratio between said fifth PMOS transistor and said first NMOS transistor of about 4:1, respectively. The limitation was not found in the collected prior art of the reference.

Regarding Claim 12, the claim introduces into the circuit two additional CMOS stages and capacitance. The closest reference for the claim is Maloney et al. (US 6,510,033), which discloses the circuit similar to that of the claim. However, the reference cannot be used due to a lack of appropriate motivation.

Regarding Claim 16, the claim uses, inter alia, a limitation of "the area of the rectangular shape is determined by the number of contacts needed to pass a target current". Such limitation was not found in the prior art of the record. This limitation is recited again in Claim 21.

5. Conclusion

The prior art made of record not relied upon is considered pertinent to applicant's disclosure: US 6,510,033, US 6,385,028, US 5,436,183, US 5,946,177, US 5,117,129.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (703) 305-0759. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone numbers for organization where this application or

proceedings is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Z.K.
07/18/2003

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800